A Grid Current-controlling Shunt Active Power Filter

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Abstract— In this paper, the implementation of a three-phase shunt active power filter is presented. The filter is essentially three independent single-phase current-controlled voltage source inverters (CC-VSI) with a common DC bus. The CC- VSI is operated to directly control the AC grid current to be sinusoidal and in phase with the grid voltage. The APF consists of a current control loop, which uses polarized ramptime current control and a voltage control loop, which employs a simple Proportional Integral control. The experimental results indicate that the active filter is able to handle predominantly the harmonics, as well as the unbalance and reactive power, so that the grid currents are sinusoidal, in phase with the grid voltages and symmetrical.

I. INTRODUCTION

Non linear loads, especially power electronic loads, generate harmonic currents and voltages in power systems. They cause a low power factor, increase the losses and reduce the efficiency of the power system, and lead to voltage distortion. Passive LC filters can be used to eliminate harmonic currents. However, bulk passive components, series and parallel resonance, a fixed compensation characteristic are the main disadvantages of passive filters. To overcome passive filter problems, for many years, various active power filters (APF) have been developed [1][2][3].

Conventionally, the power inverter as a shunt APF is controlled in such a way as to inject equal-but-opposite harmonic and reactive compensation currents based on calculated reference currents. Hence, the current sensors are installed on the load side. Then, their output signals will be processed to construct the reference or desired currents, which consist of harmonic and reactive components as well as negative- and zero-sequence components for unbalance compensation. Once the desired reference currents have been established, the currents must be injected into the grid accurately using the power inverter with a current control mechanism. The actual inverter currents must attempt to follow the harmonic-rich reference currents.

However, the construction of a reference current waveform will introduce distortion or inaccuracies due to filter and extensive calculations with inherent delays and errors. Furthermore, load or power system changes take time to be included by the reference current waveforms. Hence, the reference current created for the inverter current will have not only significant steady-state error, but also transient error. The distortion and inaccuracies can be significantly reduced if these computational, filtering and control problems could be avoided. Therefore, in this paper, the idea of directly controlling the grid/source current to track a three-phase balanced sinusoidal reference current rather than the inverter current to follow the harmonic-rich reference current using a current controller will be presented. In addition, for selection of a current control technique, capability of minimizing ripple current using a fixed switching frequency technique is greatly desirable so that there is no additional error. Hence, polarized ramptime current control (PRCC) based on zero average current error (ZACE) will be chosen for this application.

II. ACTIVE FILTER CONFIGURATION

The three-phase shunt active power filter is a three-phase four-wire current-controlled voltage-source inverter (CC-VSI) with a mid-point earthed split capacitor (C_1 and C_2) in the DC bus and inductors (L_{inv}) in the AC output. The APF consists of two control loops, namely a current control loop and a voltage control loop. The current control loop is PRCC that shapes the grid currents to be sinusoidal by generating a certain pattern of PWM for continuous switching of the inverter switches. The voltage control loop is a simple Proportional Integral (PI) control to keep the DC-bus voltage constant and to provide the magnitude of reference current signals. Fig. 1 describes the shunt active power filter configuration.

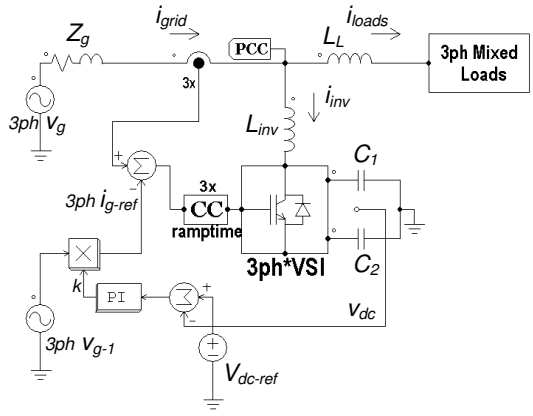

Fig. 1: Shunt active power filter configuration

A. Series Inductance

Another component of this system is a series inductance L_L, which value of the reactance X_L is comparable to the effective

grid impedance, Z_g [4][5]. Basically, the inductor provides the required voltage decoupling between load harmonic voltage sources and the grid. It also enhances the controllability of the current controller by reducing the current slope of the loads.

Without a series inductor, the point of common coupling (PCC) is tied to the load harmonic voltage source. The load harmonic voltage considerably characterizes the harmonic voltage at the PCC. As a result, there would still be harmonic voltages across the grid impedance, which would continue to produce harmonic currents and could not be compensated for by a shunt APF. Currents from the shunt APF do not significantly change the harmonic voltage at the loads.

With a series inductor, for a sinusoidal grid current, the CC-VSI output current is equal-but-opposite to the unwanted load current. These two currents generate identical harmonic voltages across the series inductance and the inverter inductance (in relative proportion to the inductances). In doing so, the CC-VSI generates the output harmonic voltage, which is equivalent to the load harmonic voltage. For perfect filtering, when no harmonic current flows through the grid impedance, a combination of the inverter and the load will be seen as infinite impedance for the grid harmonic voltages. The circuit equivalent from the harmonic point of view is shown in Fig. 2.

If a fundamental grid current component flows through the grid impedance, the voltage across the grid impedance will also be a fundamental component. The voltage across the grid impedance is represented by the $jI_{g\text{-}1}X_g$ phasor (assuming the resistance is negligible). With the $V_{g\text{-}1}$ (the fundamental component of the grid voltage) fixed, the grid harmonic voltage $V_{g\text{-}h}$ is represented in vector form by a circular region added to $V_{g\text{-}1}$. The voltage at the PCC (V_{pcc}) can be illustrated in Fig. 3. Hence, any harmonic voltage at the PCC actually mirrors the grid harmonic voltage. For a harmonic-free grid voltage, the voltage at the PCC only contains a fundamental component.

B. Direct Control of the Grid Current

As seen from Fig. 1, a node, which is a point of common coupling (PCC), is created with three connections, one each to the load, the grid and the inverter. Accordingly, all three currents – i_L, i_g, and i_{inv} – (for three or four wires) are potentially accessible to be directly controlled by the CC-VSI, following the basic current summation rule:

$$i_g = i_{inv} + i_L \tag{1}$$

Thus, for the CC-VSI operated to directly control the grid current, the current sensors are located on the grid side. The grid current is sensed and directly controlled to follow a symmetrical sinusoidal reference signal, which is in phase with the grid voltage. For perfect tracking, the shunt APF automatically provides the harmonic, reactive, negative- and zero-sequence currents for the load according to (1) without measuring and determining the unwanted load current components. Hence, the shunt APF has also the ability to balance the asymmetrical currents.

Moreover, the controllability of the grid current can be achieved using bipolar PWM switching. The upper and lower power switches of each half-bridge are switched on a complementary basis. As a result, the inverter output current, as well as the grid current, can always be controlled to ramp up and down continuously. Therefore, the direct control of the grid current is feasible because the switching action will have a direct, immediate and predictable effect on the AC grid current, and hence provide the controllability.

By directly controlling the grid currents, the shunt APF can provide complete compensation for many loads at the PCC instead of compensating for each load individually. The system is simple and efficient because only one current sensor per phase is required, located on the grid side.

In addition, controlling the grid current rather than the inverter current allows us to create a sinusoidal current reference (for the grid current), rather than having to create a harmonic- and transient-rich current reference (for the inverter current). The idea to obtain the desired grid current waveform instantaneously without calculation is easily fulfilled by using an active power balanced technique. The active power is maintained balanced among the grid, the load and the DC bus of the power inverter.

III. THE CURRENT CONTROL LOOP

In the current control loop, the current sensors on the grid side detect the grid currents. The outputs of the sensors are compared to the three-phase symmetrical sinusoidal reference signals, which are in phase with the grid voltages. The current error signals, which are the differences between the actual currents (grid currents – i_g) and the reference signals – $i_{g\text{-}ref}$, are processed using polarized ramptime current control (PRCC) to generate PWM signals. The pulse signals drive the switches so that the VSI produces currents for compensation.

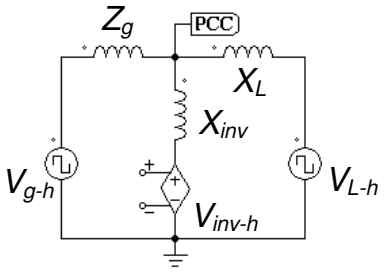

Fig. 2: Circuit equivalent for harmonics

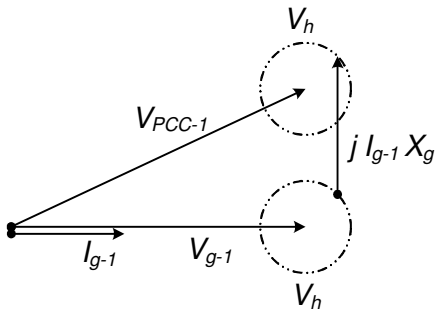

Fig. 3: Phasor diagram of voltages at the PCC for successful compensation

The PRCC technique has an important role in enhancing the performance and effectiveness of the filter to control the current loop of the CC-VSI. The operation principle of PRCC is based on ZACE (zero average current error) [6][7]. The current error signal is forced to have an average value equal to zero with a constant switching frequency. The PRCC maintains the area of positive current error signal excursions equal to the area of negative current error signal excursions, resulting in the average value of the current error signal being zero over a switching period (Fig. 4). The switching period (or frequency) is also kept constant based on the choice of switching instants relative to the zero crossing times of the current error signal. The PRCC has a high bandwidth with a fast transient response that can quickly follow the rapid changes in non linear loads.

In order to observe the current-control operation, the single-phase equivalent circuit as shown in Fig. 5 is examined.

A. *Operating condition requirement*

Neglecting the losses in the inverter, the output current for each phase of the inverter through the inductance L_{inv} can be expressed in a switching function (s) as:

$$\frac{di_{inv}}{dt} = \frac{1}{L_{inv}}(v_{pcc} - s\,v_{C1} - (s-1)\,v_{C2}) \tag{2}$$

s = 1 if the upper switch is closed, and s = 0 if the upper switch is open. It must be assumed that v_{pcc}, v_{C1} and v_{C2} are constant over the switching period. The switches are operated on a complementary basis. For $\frac{di_{inv}}{dt} > 0$, then

$$v_{pcc} - s\,v_{C1} - (s-1)\,v_{C2} > 0 \tag{3}$$

To satisfy this condition, the relationship between DC-capacitor voltages and the voltage at the PCC in terms of the switching function is given by:

If s = 1, then $v_{C1} < v_{pcc}$
If s = 0, then $-v_{C2} < v_{pcc}$ (4)

Values of v_{C1} and v_{C2} are always positive. For s = 1, the system does not work during the negative half-cycle of v_{pcc}. For s = 0, any value of v_{C2} will satisfy (4) during the positive half-cycle of v_{pcc}. For the negative half-cycle of v_{pcc}, the inverter functions well, as long as $|v_{C2}| > |v_{pcc}|$.

For $\frac{di_{inv}}{dt} < 0$, then

$$v_{PCC} - s\,v_{C1} - (s-1)\,v_{C2} < 0 \tag{5}$$

To satisfy (5), the relationship between the DC-capacitor voltages and the voltage at the PCC in terms of the switching function is given by:

If s = 1, then $v_{C1} > v_{pcc}$
If s = 0, then $-v_{C2} > v_{pcc}$ (6)

In this case, the system is unlikely to be operated at s = 0 during the positive half-cycle of v_{pcc}. For s = 1 during the negative half-cycle of v_{pcc}, any value of v_{C1} will satisfy (6). During the positive half-cycle of v_{pcc}, the inverter functions well as long as $|v_{C1}| > |v_{pcc}|$.

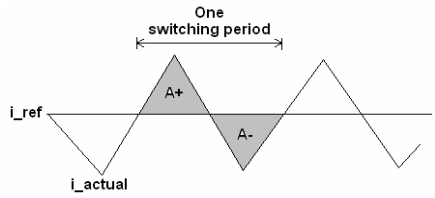

Fig. 4: Zero average current error (ZACE)

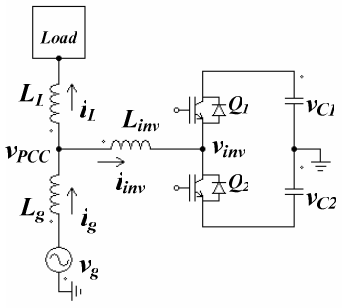

Fig. 5: Single-phase equivalent circuit

Therefore, for both cases, the inverter always generates currents as long as the magnitude of both DC-capacitor voltages (v_C) is greater than the peak value of the PCC voltage ($v_{pcc\text{-}peak}$). If this condition is not achieved, then the required operating condition for the system is not provided, and the compensation fails completely.

B. *Controllability condition*

The PRCC has characteristics similar to a sliding mode control [6][8]. Therefore, the current error signal ε, which is a controlled parameter, can be defined as a sliding surface.

$$\varepsilon = i_g - i_{g\text{-}ref} \tag{7}$$

To ensure that the system can remain on the sliding surface and maintain perfect tracking, the following condition must be satisfied:

$$\varepsilon\,\dot{\varepsilon} \le 0 \tag{8}$$

where $\dot{\varepsilon}$ is derived from (7):

$$\frac{d\varepsilon}{dt} = \frac{di_g}{dt} - \frac{di_{g-ref}}{dt} \tag{9}$$

From the switching operation implementation, the $\dot{\varepsilon}$ is able to be controlled such that a positive value of the error signal produces a negative derivative of the error signal ($\dot{\varepsilon} < 0$), and a negative value of the error signal produces a positive derivative of the error signal ($\dot{\varepsilon} > 0$). Controlling the sign of $\dot{\varepsilon}$ is associated with controlling the sign of di_g/dt to be positive or negative.

Referring to the filter operation by controlling the grid currents, and combining (1) and (9), $d\varepsilon/dt$ can be expressed as:

$$\frac{d\varepsilon}{dt} = \frac{di_L}{dt} + \frac{di_{inv}}{dt} - \frac{di_{g-ref}}{dt} \tag{10}$$

Since the sign of di_{inv}/dt and di_g/dt are matching, perfect tracking can be achieved when:

$$\left|\frac{di_{inv}}{dt}\right| > \left|\frac{di_L}{dt} + \frac{di_{g-ref}}{dt}\right| \quad (11)$$

As long as equation (11) is not satisfied, then the system is moving away from the sliding surface, and the CC-VSI loses its controllability. This means that zero crossing of the current error signal will not occur at the end of a half-switching period, since by definition, the system is controllable if there exists a (piecewise continuous) control signal that will take the state of the system from any initial state to any desired final state in a finite time interval [9]. Refer to (2), di_{inv}/dt is normally determined by L_{inv} dan capacitor voltages.

IV. THE VOLTAGE CONTROL LOOP

In order to satisfy the operating condition requirement of the current control loop, the DC-capacitor voltages have to be forced greater than $v_{pcc\text{-}peak}$. In addition, the DC-bus voltage has to be kept constant by regulating the active power balance of the system, and then deciding the amplitude of the grid currents. The voltage control loop employs a Proportional Integral (PI) controller to maintain the desired DC-bus voltage level.

A. *Power flow*

Power flowing in the grid, the load and the inverter is expressed in terms of real power p, imaginary power q, and zero sequence power p_0 [10][11][12], which consist of an average value and an oscillating value.

Considering a non-sinusoidal and unbalanced system, the load power can be decomposed into:

$$\begin{aligned} p_L &= \bar{p}_L + \tilde{p}_L \\ q_L &= \bar{q}_L + \tilde{q}_L \\ p_{L-0} &= \bar{p}_{L-0} + \tilde{p}_{L-0} \end{aligned} \quad (12)$$

Due to successful compensation for the unwanted currents of the load, the grid currents will be sinusoidal, balanced and in-phase with the grid voltages. As a result, if the grid voltage is non-sinusoidal and/or unbalanced, the powers p_g, q_g and $p_{g\text{-}0}$ generated from the grid become:

$$\begin{aligned} p_g &= \bar{p}_g + \tilde{p}_g \\ q_g &= \tilde{q}_g \\ p_{g-0} &= 0 \end{aligned} \quad (13)$$

The power developed by the inverter is calculated by subtracting the power supplied by the grid and the power consumed by the load, given by:

$$\begin{bmatrix} p_{inv} \\ q_{inv} \\ p_{inv-0} \end{bmatrix} = \begin{bmatrix} \bar{p}_g - \bar{p}_L \\ -\bar{q}_L \\ -\bar{p}_{L-0} \end{bmatrix} + \begin{bmatrix} \tilde{p}_g - \tilde{p}_L \\ \tilde{q}_g - \tilde{q}_L \\ -\tilde{p}_{L-0} \end{bmatrix} \quad (14)$$

From (14), the inverter controls the whole imaginary power associated with the load $\bar{q}_L + \tilde{q}_L$ and the grid $\tilde{q}_g$ (in a small value). However, the DC bus does not contain imaginary power. The CC-VSI generates q_{inv} but it does not flow out of or into the DC-bus capacitors. According to Watanabe [11] and Peng [12], the imaginary power circulates among the phases due to the switching of the inverter. In other words, instantaneously, the imaginary power required by one phase can be supplied by the other phase.

For the average value $\bar{p}$ of the real power, the inverter supplies the zero sequence average (active) power $\bar{p}_{L-0}$ needed by the load. To supply the load zero sequence active power, the inverter has to take an active power from the grid because the inverter has no DC source. Neglecting the losses in the power converter, in steady state, the active power consumed by the load is equal to the active power supplied by the grid, and total active power flowing to the inverter is zero. The active power balance according to (14) can be stated as: $\bar{p}_{inv} + \bar{p}_{inv-0} = \bar{p}_g - \bar{p}_L - \bar{p}_{L-0} = 0$. Thus, the active power taken from the grid by the inverter, which is used to support the zero sequence power delivered to the load, is: $\bar{p}_{inv} = \bar{p}_g - \bar{p}_L = \bar{p}_{L-0}$. Additional active power consumption is required to compensate for the losses, so that $\bar{p}_{inv} = \bar{p}_{L-0} + \bar{p}_{loss}$. The active power balance is regulated by the voltage control loop to retain the DC-bus voltage around its reference level.

The inverter supplies $\tilde{p}_L$ as well as $\tilde{p}_{L-0}$ and consumes $\tilde{p}_g$ (in a small value) using DC capacitors as an energy storage element. The DC capacitors absorb (release) energy when $\tilde{p}$ is positive (negative). This power does not affect the DC-bus voltage level since its mean value equals to zero. However, it will appear in the DC-bus voltage as a ripple. The ripple becomes small if the value of DC capacitors is high.

B. *DC-bus voltage control system*

For successful compensation, the grid current is the same as its reference. To obtain the reference signal, only one phase of the three-phase grid voltage is detected as the reference phase. Afterwards, a three-phase symmetrical sinusoidal waveform is generated using a phase lock loop (PLL) circuit. Only the magnitude of the grid current needs to be determined.

As mentioned above, in steady state and ignoring the losses, the active power consumed by the load is equal to the active power supplied by the grid, and $\bar{p}_{inv}$ will be zero. With no power flow into the inverter, the average DC-bus voltage thus can be maintained at the reference voltage level.

When a load variation occurs, the active power balance between the load and the grid will cease to be maintained. The inverter immediately supplies (absorbs) the active power mismatch between the grid and the load, since the voltage control loop cannot respond instantaneously to provide the appropriate grid reference current magnitude. This yields a DC-bus voltage deviation (ΔV_{dc}).

Due to active power balance, the amplitude of grid active currents must be adjusted appropriately to compensate for the active power charged/discharged from DC capacitors of the inverter. The required change in grid currents will come as soon as the voltage control loop responds to change (increase or decrease) in the magnitude of the grid currents. The output of the PI controller, which is a gain k, can determine the amount of ΔV_{dc} that corresponds to the grid current amplitude (Fig. 6). The total active power flowing to the inverter will go

to zero when the grid current amplitude approaches its final value. The average DC bus voltage is then recovered and stays at the reference voltage. Finally, the active power supplied from the grid is matched to that consumed by the load. A new steady state has been achieved with a new grid current amplitude. Hence, the sinusoidal grid current reference signal is given by:

$$i_{g\text{-}ref} = k\, v_{grid\text{-}1} \tag{15}$$

where $v_{grid\text{-}1}$ is the fundamental component of the grid voltage, and obtained from a phase-lock-loop (PLL) circuit detecting the grid voltage. The value of k is obtained from the output of a simple PI controller in an voltage control loop regulating the CC-VSI DC-bus voltage.

The voltage control loop block diagram is shown in Fig. 6. Considering a perfect tracking current control loop, the grid current is the same as its reference. The inverter DC-bus voltage is detected and reduced by a gain K_f to the level of a signal. Since the DC-bus voltage contains ripples, a first-order low-pass filter (LPF) is added to the feedback loop to obtain a smooth gain k. The output of the PI controller, which is a gain k, is multiplied by $v_{g\text{-}1}$, which is the fundamental component of the grid voltage obtained from a PLL circuit and then used as a reference waveform. The inverter currents will flow through the switches to the DC capacitors to develop the DC-bus voltage. K_C is a power conversion factor between the AC side and the DC side of the power converter.

V. THE THREE-PHASE SHUNT ACTIVE POWER FILTER FOR MIXED LOADS

The system in Fig. 1 is tested using laboratory experiment to verify the shunt APF concepts. The three-phase grid voltages contain harmonics, and the mixed loads consist of single- and three-phase linear and non-linear loads. The linear loads are resistive and inductive loads, while the non-linear loads are a rectifier type of loads. The loads represent the distributed linear and non-linear loads, which exist in a typical electrical distribution system such as in commercial buildings. The three-phase current waveforms along with their harmonic spectrums of the mixed loads, as well as the neutral current from the laboratory experiment, are shown in Fig. 7. It shows clearly that the currents are not sinusoidal. The load phase-currents are also unbalanced and contain reactive components. The significant third-harmonic current flows in the neutral wire.

Fig. 8 demonstrates the steady-state performance of compensation results. It can be seen that the shunt APF is successfully able to compensate for the total mixed loads. Although the grid voltage contains harmonics, it does not distort the grid currents. The PRCC can force the grid currents to follow accurately the sinusoidal reference waveforms without additional low order harmonics. The grid currents become both sinusoidal and in phase with the grid voltages (with insignificant phase leading by approximately 5° due to AC filter capacitors (C_{ac}) – in Fig. 9, only phase A of the grid voltage is shown). The amplitude is determined by the active power required by the system. The PRCC VSI is capable of controlling the low order harmonics due to ZACE with a fixed switching frequency. However, it produces a high frequency switching current ripple. To avoid the current ripple flowing to the grid, small AC filter capacitors (C_{ac}) are installed on the grid side.

After compensation, the grid currents are symmetrical both in magnitude and phase. As a result, the neutral current at the grid is also reduced to zero. The grid currents are balanced because the CC-VSI is able to force the grid currents to follow a three-phase balanced sinusoidal reference signal. Then, the inverter creates the inverse of the negative- and zero sequence currents automatically to balance the unbalanced loads, without measuring and determining the negative- and zero sequence components. From Fig. 10, it is obvious that the CC-VSI is able to generate three different currents for each phase as well as the neutral current. Hence, the inverter not only generates harmonics to eliminate the load harmonics but also provides balancing to create the symmetrical grid currents.

VI. CONCLUSION

This paper explains the implementation of a three-phase four-wire shunt active power filter (APF) operated to directly control the AC grid current to be sinusoidal and in phase with the grid voltage. By doing this, the three-phase shunt APF automatically provides compensation for harmonics, reactive power and unbalance without measuring/sensing the load currents. The computational, filtering and control problems can be avoided so that the distortion and inaccuracies problems can be significantly minimized. The experimental results prove the validity of the concept.

The polarized ramptime current control (PRCC) is very effective to shape the grid to be sinusoidal without additional low order harmonics due to the concept of zero average current error (ZACE) with fixed switching frequency. Thus, it is suitable for the grid current-controlling shunt APF.

There are many advantages to directly control the grid current. Firstly, it is easy to create a simple sinusoidal reference for the grid current using the active power balance method. The reference current is an appropriate reference to minimize the grid harmonic currents. Secondly, the grid currents produced will be sinusoidal, balanced and in phase with the grid voltage regardless of grid voltage conditions. Thus, it prevents (more) pollution of the electrical system from non-linear loads. Moreover, the control mechanism becomes very simple.

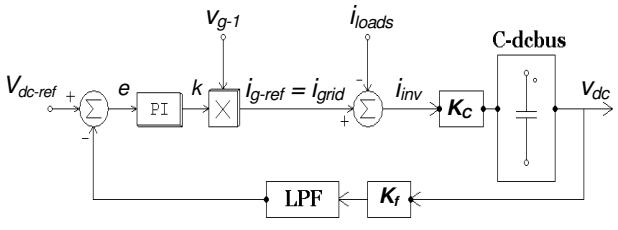

Fig. 6: Voltage control loop

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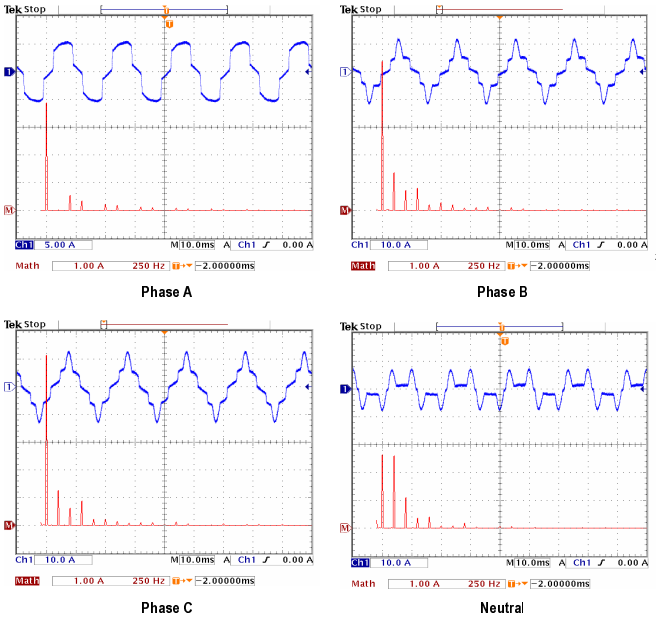

Fig. 7: phase and neutral currents for mixed loads

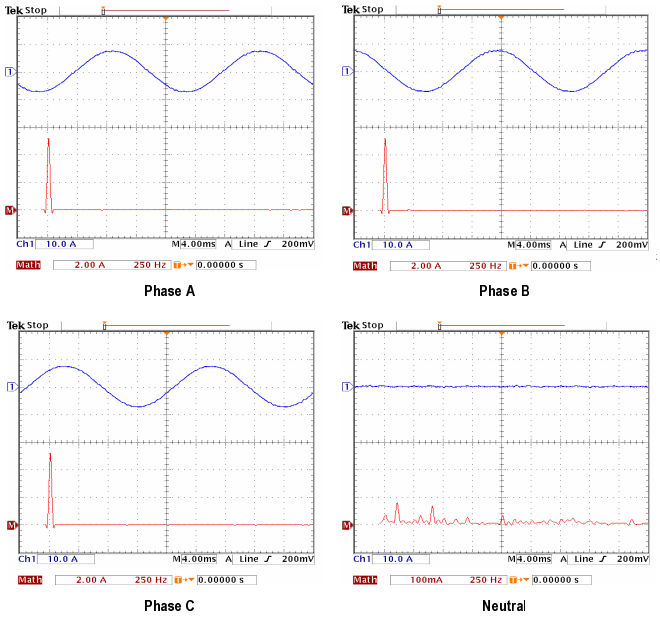

Fig. 8: phase and neutral currents of the grid after compensation

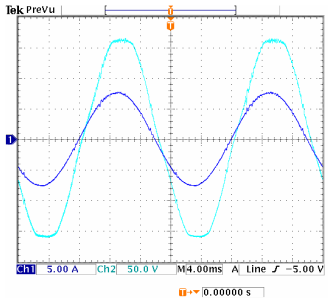

Fig. 9: phase-A grid voltage and current after compensation

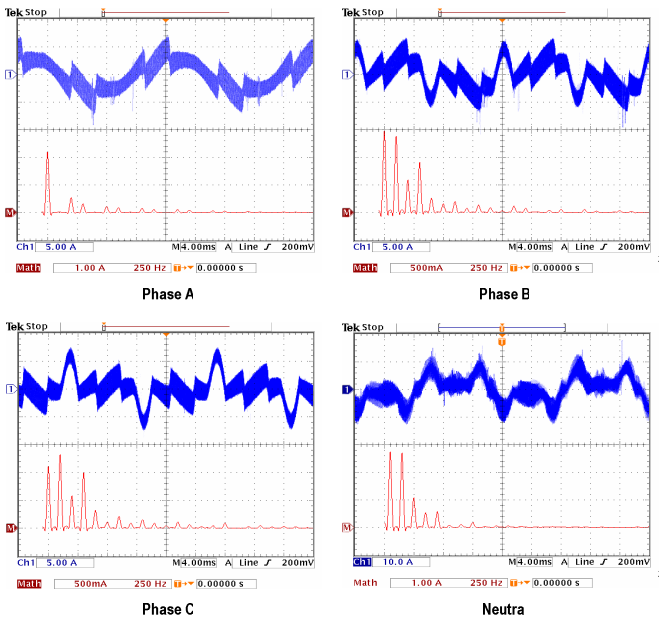

Fig. 10: phase and neutral currents of the CC-VSI